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REMARKS

Claims 1-11 and 14-21 remain in the application.

In a voicemail of August 15, 2002, Examiner Renzo Rocchegiani imposed a restriction requirement between the method of Claims 1-11 and the apparatus of Claims 12 and 13. Applicants elect the method of Claims 1-11. The non-elected claims are canceled.

In a telephone conference on August 19, 2002, the Examiner agreed that a Preliminary Amendment incorporating the election could be submitted by facsimile within a few days thereafter. The amendments correct many editorial errors in the description and claims, remove unnecessary limitations, and add a broader set of claims.

In view of the above amendments and remarks, consideration and allowance of all claims are respectfully requested. If the Examiner believes that a telephone interview would be helpful, he is invited to contact the undersigned attorney at the listed telephone number, which is on California time.

Respectfully submitted,

Date: 21 August 2002

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Version with markings to show changes made

In the specification:

Two Paragraphs at page 2, line 14 to page 3, line 15:

Conventionally, the inter-level dielectric layers have been oxide layers formed of silica of the approximate composition SiO_2 or related silicate glasses such as borophosphosilicate glass (BPSG). However, these materials have a relatively high dielectric constant k of about 3.9 but even with process variations the value is limited to $k<4.0$. In view of the increased operating frequencies of advanced integrated circuits and the reduced spacing between conductive features, such as buses, there has been much recent development in low-k inter-level diclectric materials having reduced dielectric constants of less than 3.9. Doped silica such as fluorosilicate glass (FSG) has a dielectric constant of somewhat over 3. Other low-k dielectrics are being developed based either on silicon or carbon, but almost all of which can be characterized as oxides. Many of these low-k dielectric materials, particularly those having ultra low dielectric constants of $k<2.2$, have a stability problem relative to silica in that, upon being exposed to air, they absorb or react with water vapor, with a resultant increase in the dielectric constant. The problem is particularly acute when a partially fabricated wafer having an exposed low-k dielectric layer is moved from one processing platform to another. Not only in most production lines [line] is the dielectric material exposed to air as a wafer bearing cassette is manually moved between platforms, but the duration of the exposure can both be long and be of varying lengths because of variable processing queues and other fabricational uncertainties such as work shift changes and equipment maintenance and breakdown and repair.

One conventional fabrication method of fabricating a of a dual-damascene inter-level dielectric structure and its metallization will be described with reference to several cross-sectional views of the developing structure. This particular exemplary method is generally referred to as "via first" dual damascene. As illustrated in FIG. 1, a lower-level dielectric layer

10, possibly of a low-k dielectric material, includes a copper feature 12 recessed in its surface. A thin barrier layer 14, also acting as an etch stop layer, and an upper level dielectric layer 16 are deposited over the lower-level dielectric layer 10 and its copper feature 12. The barrier layer may be formed of silicon nitride (SiN_x, where x may range between 1 and 1.5), BLOk™ (available from Applied Materials of Santa Clara, California), carbon rich nitride , silicon carbide, [caribide] or a spin-on dilectric. Exemplary nitride thicknesses are 20 to 100nm. This layer is generally referred to as stop layer 1. Optionally, a second stop layer 19 is provided to delineate [deliniate] the bottom of the trench.

Paragraph at page 5, lines 5-10:

Thereafter, in steps not directly relevant to the invention, copper is filled into the hole, preferably by electrochemical plating (ECP). The copper seed layer 34 acts [as] both to nucleate the copper deposition and as an electrode for ECP. The dual-damascene structure has the advantage that the ECP copper deposition is deposited to not only fill the etched hole but also to extend over the field area 34 at the top of the upper dielectric layer 16. Chemical mechanical polishing (CMP) removes the copper outside the etched hole but stops on the harder oxide on the field area 34 outside of the trench 26.

Paragraph at page 6, lines 16-21:

According to one embodiment, an integrated process includes etching an oxide layer or a barrier and sputtering or CVD depositing metal and metal barrier layers on [one] a single mainframe. Separate plasma processing chambers are connected to the mainframe through respective slit valves allowing the vacuum levels in the stages to be maintained independently of the processing pressures. Substrates are passed between the stages through gated passages allowing different vacuum levels to be maintained throughout processing of many substrates.

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Paragraph at page 10, lines 14-19:

Various types of plasma etch reactors are commonly used for oxide etching and can be used as the plasma etch reactor 106. Two exemplary reactors are a magnetically enhanced reactor (MERIE) and an inductive decoupled [decouples] plasma reactor. An example of the MERIE type is the eMAX™ oxide etch reactor available from Applied Materials, while an example of the inductive type is the IPS™ oxide etch reactor also available from Applied Materials.

Paragraph at page 12, lines 4-10:

Each of the metallization reactors is selectively isolated from the transfer chamber 100 by a respective slit valve to isolate the transfer chamber 100 from the process environment and is also pumped by a separate respective pumping system. As a result, between the sputter operations performed in the metallization chambers, the exposed metal surfaces are not exposed to significant oxygen or humidity. After completion of the liner layer deposition, the two robots 122, 102 pass the wafer to the load lock, and the wafer is returned to one of the cassettes 76, 78 on [in] the loading tables 72, 74.

Four paragraphs at page 13, line 9 to page 14, line 3:

The process may begin with a masked wafer, for example, either the structure of FIG. 1 or FIG. 9. In step [400] 40, the wafer is moved from the load lock into the first transfer chamber and, if necessary, is oriented in step [420] 42. Thereafter, steps 44-48 [440-480] are performed in chambers that are connected to the first transfer chamber. [Theses] These steps are referred to as etching steps 52' [520] which do not require the high vacuum levels of the metallization chambers. Again, clean step 50 [500] is shown as optional.

In step [540] 54, the wafer is degassed. The degassing may be performed in the higher-pressure stage 52 [520] or in a separately pumped intermediate load lock [load locks] between the two pressure stages. At this point, the wafer has a fully etched via hole with no

barrier layers. Therefore, both the oxide and the underlying copper feature are exposed. In step [560] 560, the wafer is transferred from the degassing station to the second, lower-pressure [,] transfer chamber. In step [580] 58, the metal barrier is deposited and in step 60 a copper seed layer is deposited. Steps [580] 58 and [600] 60 for depositing metal liner constitute a lower-pressure sequence 62' [620] performed in reactors associated with the lower-pressure transfer chamber.

Finally, in step [640] 64, the wafer is transferred from the lower-pressure transfer chamber back to the load lock, typically through the higher-pressure transfer chamber.

The staged-vacuum process described above is advantageous in that the dirtier etching and cleaning processes as well as the dirty incoming wafer and its photoresist mask are confined to the higher-pressure transfer system while the sputtering processes, which require [requires] a high vacuum, and the processes in which metal is exposed are isolated in the low-pressure stage. Tepman et al. have described a staged-vacuum sputtering platform in U.S. Patent 5,186,718. The exposure of metal to oxygen can be further reduced by performing the barrier strip 48 [480] in the low-pressure stage 62' [620] rather than the high-pressure stage 52' [520].

Six Paragraphs at page 15, lines 1 to page 16, line 19:

Separate vacuum pumping systems are provided for at least the oxide etch reactor 106 [1000] and the ash/strip reactor 108 so as to allow the first transfer chamber 1000 to always be maintained at a pressure below 1 Torr. As a result, as the wafer is being passed between reactors and to the next stage, it is never exposed to substantial air or humidity.

A separate degas station 110 [1110] may also be coupled to the first transfer chamber 1000 to heat the stripped wafer to remove as much adsorbed oxygen or other gases before the robot 102 [1000] transfers the degassed wafer to on of two platform pass through chambers 1120, 1140 arranged in parallel between the first, higher-pressure central transfer chamber 100 and a second, lower-pressure (high vacuum) central transfer chamber 1200. A vacuum pumping system attached to the second central transfer chamber 1200 is capable of maintaining it at a pressure of

no more than 10^{-6} Torr, and preferably no more than 10^{-8} Torr. The latter pressure is that associated with sputtering reactors. Each of the platform pass through chambers 1120, 1140 has its own vacuum pumping system and a pair of selectively openable slit valves between it and the two transfer chambers 1000, 1200. Thereby, the wafer may b e passed from the first low vacuum transfer chamber 1000 to the second, high vacuum transfer chamber 1200 without degrading the strong vacuum of the latter. It is also possiblc to attach a processing station, such as a prcclean or a degassed, to one of the platform pass through chambers 1120, 1140.

A second dual-blade robot 122 [1220] located in the second transfer chamber 1200 can transfer a wafer between either of the platform pass through chamber 1120 1120, 1140 and any of the other stations attached to the second transfer chamber 1200. The number and types of reactors associated with the second transfer chamber 1200 [120] depends upon the desired integrated circuit structure and the form of the via and its liner. However, an exemplary configuration for fabricating a copper via includes a first sputtering (PVD) reactor 1240 with a tantalum target for sputtering a Ta/TaN barrier layer and a second PVD reactor 126 [1260 for] with a copper target for sputtering a copper seed layer to produce the structure of FIG. 5. Particularly the copper PVD reactor 126 [124] is advantageously implemented with the previously mentioned SIP^{+} sputter reactor. However, other types of sputter reactors may be used. Sometimes, a sub-barrier of TiN is used. Also, in some applications, particularly with very high aspect-ratio vias, a chemical vapor deposition (CVD) is used to deposit one or more of the barrier metals or barrier nitrides.

Each of the reactors associated with the second transfer chamber 1200 is selectively isolated from it by a respective slit valve to isolate the second transfer chamber 1200 from the processing environment and is also pumped by a separate respective vacuum pumping system. Thereby, the second transfer chamber 1200 is maintained during wafer process at a pr3essure of no more than 10^{-6} Torr and preferably no more than 10^{-8} Torr. As a result, between the sputter operations performed in the chambers of the second transfer chamber, the exposed metal surface are not exposed to significant oxygen or humidity. After completion of the liner layer deposition,

the two robots 122, 102 [1220, 1020] pass the wafer through one of the platform pass through chambers 1120, 1140 to the load lock, and the wafer is returned to one of the cassettes [760, 780] 76, 78.

The other two reactors 128, 130 [1280, 1300] available on the high-vacuum stage of the Endura platform may include on or more of these additional reactors or may be a second pair of tantalum and copper PVD reactors so as to increase system throughput. Also, because the stop layer strip reactor involves a clean etching chemistry, it is possible to move it to the second, lower-pressure transfer chamber 1200, thereby assuring that the underlying copper feature is not exposed to more than 10^{-6} Torr of pressure once the silicon nitride has been removed.

A controller 132 [1320] controls the operation of the system including the load locks, the transfer chambers and other parts of the integrated platform.

Paragraph at page 17, lines 10-18:

The invention can be applied to a subset of the above described process in a process stretching from barrier removal to liner deposition, as illustrated in the flow diagram of FIG. 11. The process assumes that, as the wafer is being loaded into the integrated platform, the oxide has already been etched and the photoresist and polymer have been ashed but that the protective silicon nitride barrier layer remains at the bottom of the via hole. Hence, a higher-pressure sequence 1400 does not include the oxide etching or ashing but includes the previously described barrier strip step 48 [480] and cleaning step 50 [500], if the latter is needed. Thereafter, the process remains quite similar to that of [FIGS.] FIG. 6 or 9 with the lower-pressure sequence 62' [620] including the two sputtering steps [580, 600] 58, 60.

In the drawings:

Please amend FIGS. 9, 10, and 11 as marked on the attached copies thereof.

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In the claims:

1. (Amended) An integrated etch and metal liner process of a substrate including a dielectric layer [having a diclectric constant $k<4$] and covered with a patterned mask material, comprising the steps of:

transferring the substrate into a transfer chamber held at a first pressure below atmospheric pressure;

transferring the substrate from the transfer chamber to an etching chamber and etching according to said patterned mask material through said oxide layer to said etch stop layer to form a hole in said oxide layer;

ashing said mask material;

removing said etch stop layer exposed at a bottom of said hole;

transferring said wafer to a metallization chamber through said transfer chamber and without exposing the substrate to an atmospheric pressure;

depositing a barrier layer in said metallization chamber; and

depositing a seed layer.

5. (Amended) An integrated etch and metal liner process of a substrate including a stop layer covered with a dielectric layer [having a dielectric constant $k<4$ and] covered with a patterned mask material, comprising the steps of:

etching according to said mask through said oxide layer to said etch stop layer to form a hole in said oxide layer;

ashing said mask material;

removing said etch stop layer exposed at a bottom of said hole;

transferring said substrate [wafer] to a transfer chamber maintained at a sub-atmospheric pressure;

in a reactor coupled to said transfer chamber, depositing a barrier layer; and

in a reactor coupled to said transfer chamber, depositing a metal seed layer; [and,]

wherein said substrate [wafer] is maintained between said etching, ashing and removing steps and during said transferring steps at [a] sub-atmospheric pressures [pressure].

11. (Amended) The process of Claim 9, further comprising:

a fifth step of transferring said substrate [wafer] from said oxide etch reactor through said first transfer chamber to a plasma ashing reactor attached to said first transfer chamber; and

in said plasma ashing reactor, ashing said photoresist layer;

wherein said third step of transferring comprises transferring said substrate from said plasma ashing reactor through said first transfer chamber to said second transfer chamber.

Please cancel Claims 12 and 13.

14. (New) An integrated process performed in processing reactors connected to at least one central vacuum transfer chamber held at pressures of no more than 1 Torr, said processing reactors and said at least one central vacuum transfer station being formed on a single platform, said process comprising the steps of:

loading into said at least one central vacuum transfer chamber through a load lock a substrate having a dielectric layer covered by a patterned resist material;

in at least one etching reactor connected to said at least one central vacuum transfer chamber through a respective slit valve, etching said dielectric layer in said substrate according to said patterned resist material to form a hole therethrough and thereafter ashing said resist material;

in at least one deposition reactor connected to said at least one central vacuum transfer chamber through a respective slit valve, depositing a liner layer on sides of said hole;

wherein said substrate is not exposed to atmospheric pressure between said etching step and said depositing step.

15. (New) The process of Claim 14, wherein said liner layer includes a barrier layer and a copper seed layer.

16. (New) The process of Claim 14, wherein said at least one deposition reactor includes a sputter reactor with a copper target for depositing said copper seed layer.

17. (New) The process of Claim 14, wherein said at least one etching reactor includes an etch reactor for etching said dielectric layer and an ashing reactor for ashing said resist material.

18. (New) The process of Claim 14, wherein said at least one central vacuum transfer station includes a first central vacuum transfer chamber to which said at least one etching reactor is connected through its respective slit valve and a second central vacuum transfer chamber to which said at least one deposition reactor is connected through its respective slit valve and said platform further comprises a doubly gated vacuum passageway between said first and second central vacuum transfer chambers.

19. (New) The process of Claim 18, wherein said etching reactors includes an etch reactor for etching said dielectric layer and an ashing reactor for ashing said resist material and wherein said deposition reactor includes a first sputter reactor for depositing at least a part of a barrier layer and a second sputter reactor for depositing a copper seed layer.

20. (New) The process of Claim 18, wherein said second central vacuum transfer chamber is held at a pressure of no more than 10^{-6} Torr.

21. (New) The process of Claim 14, wherein said at least one central vacuum chamber consists of a single central vacuum transfer chamber.

INTEGRATED SYSTEM FOR OXIDE ETCHING AND METAL LINER DEPOSITION
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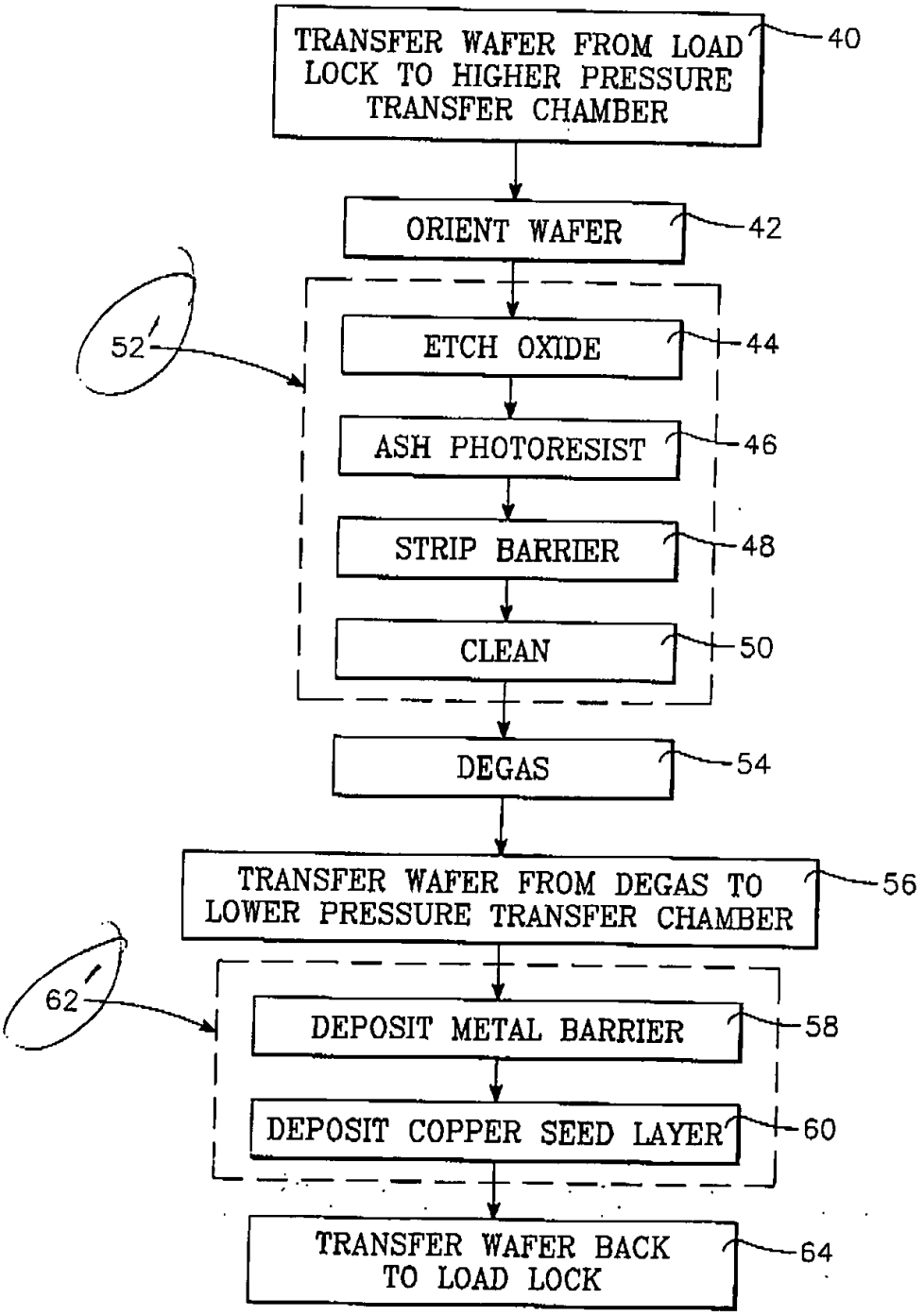

FIG. 9

INTEGRATED SYSTEM FOR OXIDE
ETCHING AND METAL LINER DEPOSITION
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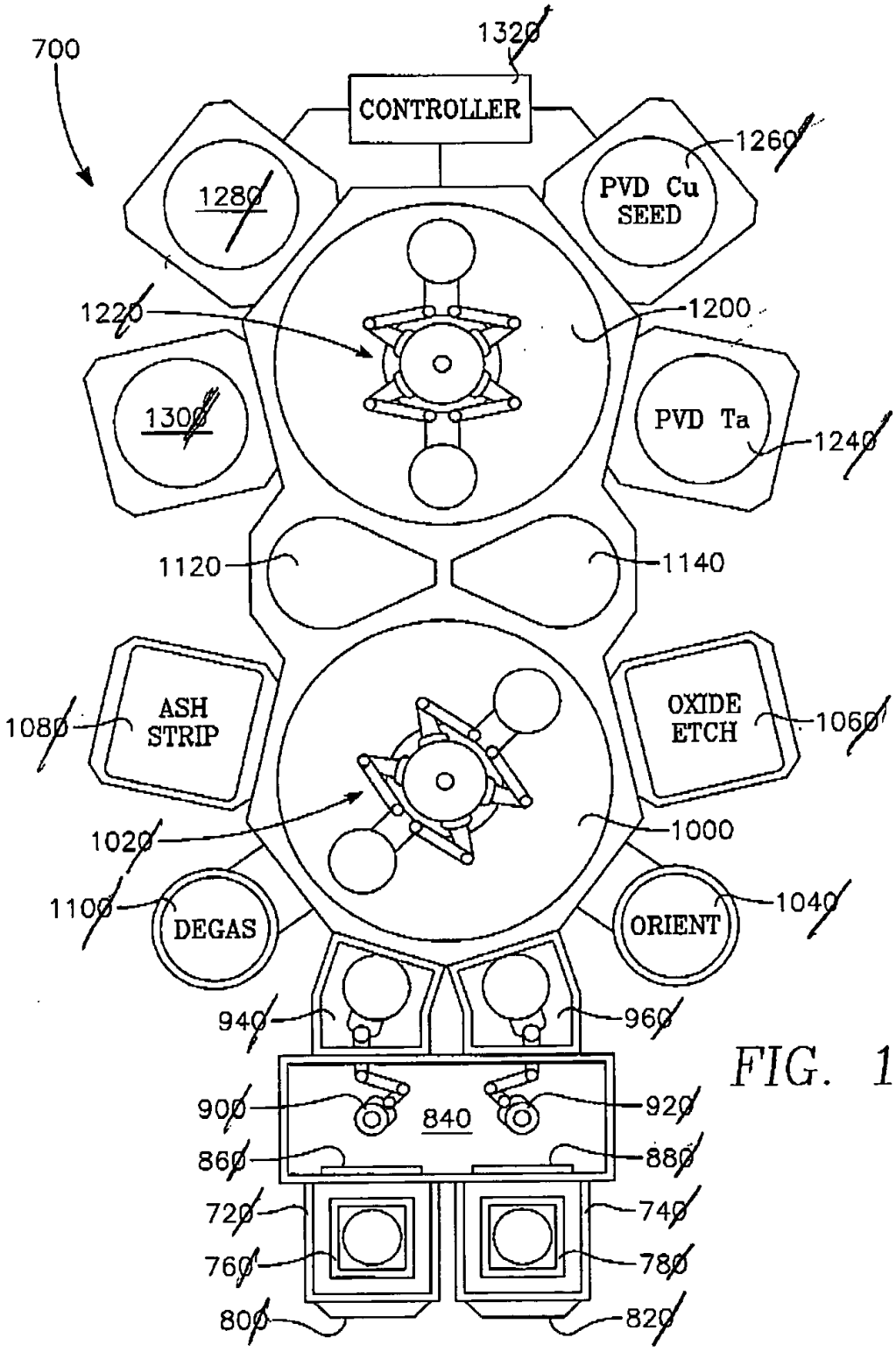

FIG. 10

INTEGRATED SYSTEM FOR OXIDE
ETCHING AND METAL LINER DEPOSITION
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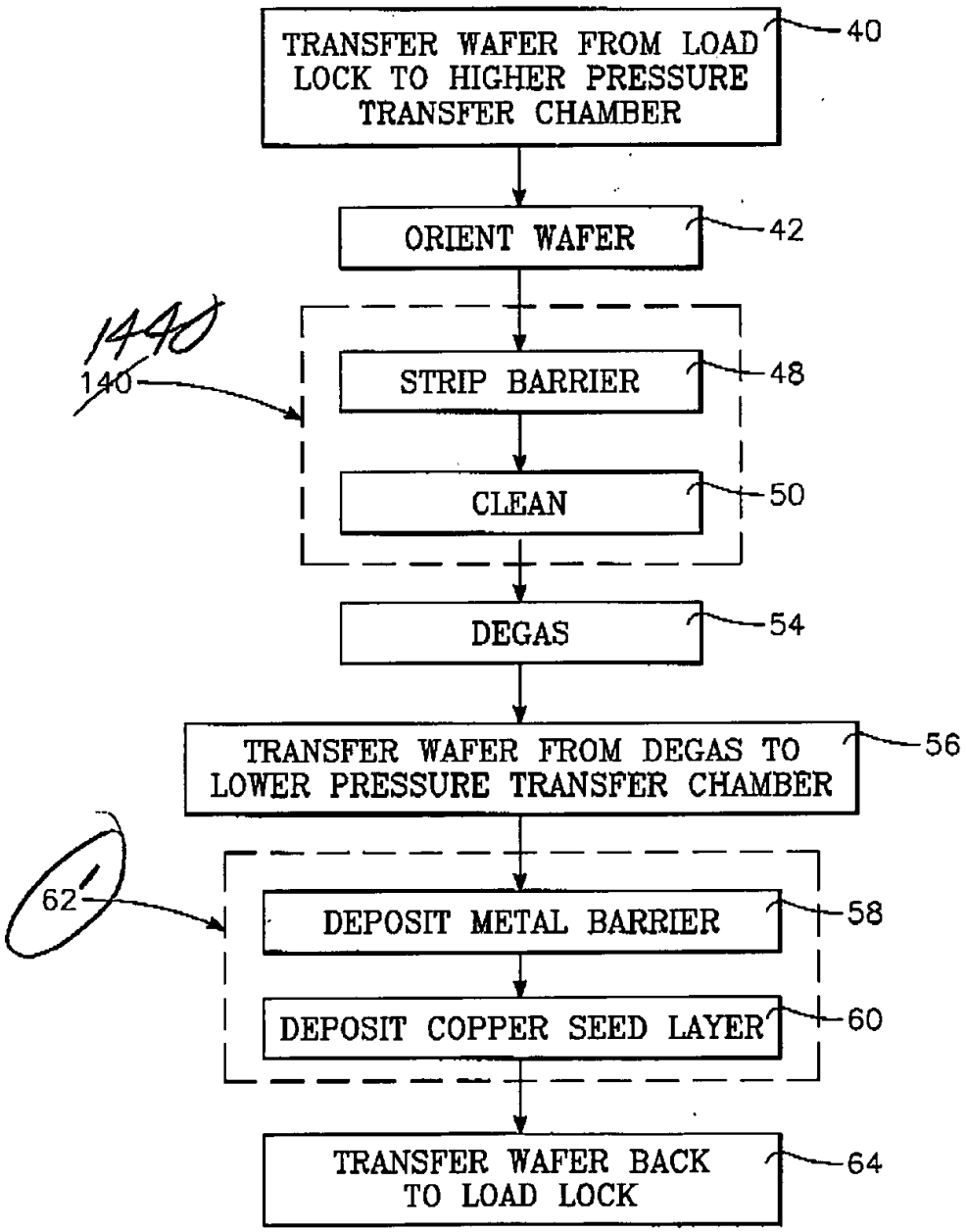

FIG. 11